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PSpice Modeling Platform for SiC Power MOSFET Modules with Extensive Experimental Validation

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***Abstract*—The aim of this work is to present a PSpice implementation for a well-established and compact physics-based SiC MOSFET model, including a fast, experimental-based parameter extraction procedure in a MATLAB GUI environment. The model, originally meant for single-die devices, has been used to simulate the performance of high current rating (above 100 A), multi-chip SiC MOSFET modules both for static and switching behavior. Therefore, the simulation results have been validated experimentally in a wide range of operating conditions, including high temperatures, gate resistance and stray elements. The whole process has been repeated for three different modules with voltage rating of 1.2 kV and 1.7 kV, manufactured by three different companies. Lastly, a parallel connection of two modules of the same type has been performed in order to observe the unbalancing and mismatches experimentally, and to verify the model effectiveness in such challenging topologies.**

Keywords—SiC-MOSFETs, PSpice modeling, Parameter extraction, Wide bandgap devices

I. Introduction

Among wide bandgap semiconductor devices, silicon carbide (SiC) MOSFETs have been experiencing a rather fast technological development process during last few years due to their promising features such as high breakdown field strength, wide bandgap, saturation velocity and thermal conductivity. In SiC high-frequency power switches, it is possible to achieve a high breakdown voltage with relatively small on-state resistance, fast switching speed, and good thermal conductivity, which allows reliable operations in harsh condition environments [1] - [6]. Moreover, not presenting tail current due to their unipolar structure, they show higher switching speed and lower losses in comparison to Silicon IGBTs and BJTs. Nevertheless, the technology used nowadays in the manufacturing of SiC MOSFETs has just settled and reliable operations are only possible for devices with quite low current ratings. For high power applications, parallel connection of several chips is required in high power modules, which are already available in the commercial market rated 100 – 800 A and 1.2 – 1.7 kV. While the technological manufacturing of SiC MOSFETs is moving toward its maturity phase, modern challenges as the reliability evaluation, and high-voltage packages development are still on their infancy stage, that hinders them to be used in the real field. On the other side, simple analytical device models are required to facilitate the power converter design, and hence to lower the development cost and effort. On this front, device modeling research is far lagging behind the technological development of SiC power MOSFETs.

Many models have been proposed in the literature to predict the static and switching characteristics of Si and SiC power MOSFETs [7] - [16], in order to support the development process of SiC-based converters and evaluate their performances and advantages. These models basically divide into two main categories: behavioral models and physics-based models. In the first typology category a mathematical fitting of the device characteristics is performed, resulting in simple equations and fast simulation time, but hardly being able to describe the device behavior in all the operating conditions. On the other hand, the physics-based ones include the physical laws governing the device, and often more complex numeric methods relying on finite-element analysis of the model. A physics-based model can estimate in a satisfactory level of detail of the MOSFET's performances, if the parameters are correctly identified, without requiring advanced knowledge of the device manufacturing features and with rather fast convergence time. The physics-based model proposed in [14] has been chosen for the purposes of this work with a novel PSpice code implementation, described in the following section. However, the use of such model to evaluate a whole module, made up of several parallelized dies, is rather new in literature and thus, verifying its validity is one of the main aims of this work.

II. Model Description and PSpice Implementation

The model presented in [13], [14] is a well-established adaptation of an IGBT model [17] to a MOSFET structure. It describes analytically a quite unique feature of the semiconductor: the presence of a sub-threshold current I_{mosl} originated at the corners of the MOSFET cells, whose effect is non-negligible at low gate voltage. This regions present lower gate threshold and transconductance respect to the main channel region.

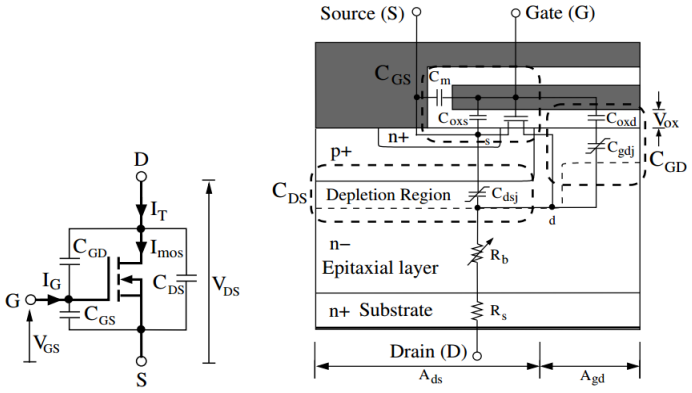

Fig. 1. Power MOSFET schematics for the McNutt-Hefner model

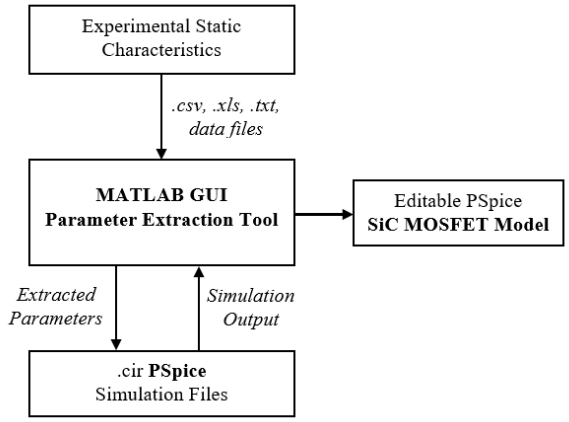

Fig. 2. Structure of the parameter extraction tool

The "soft-threshold" Vtl together with the main high-threshold Vth currents (I_{mosl} and I_{mosh}) are taken into account in two different equations, both in linear and saturation region, and then summed up to form the main MOSFET current I_{MOS} (Eq. 1 to 5 [14]). In the above equations, Kfl, Kp and Kf are the low current transconductance factor, the saturation transconductance and the linear transconductance factor, respectively, Pvf is the pinch-off voltage factor, θ is the transverse electric field parameter and y=Kf/(Kf-Pvf/2).

$$I_{mosl} = K_{fl}K_pK_f\frac{(V_{gs}-V_{tl})V_{ds}-\frac{1}{y}\left[P_{vf}^{1-y}V_{ds}^{y}(V_{gs}-V_{tl})^{2-y}\right]}{1+\theta(V_{gs}-V_{tl})} \quad (1)$$

$$when\ V_{ds} \le \frac{V_{gs}-V_{tl}}{P_{vf}}$$

$$I_{mosl} = K_{fl}K_p\frac{(V_{gs}-V_{tl})^2}{2[1+\theta(V_{gs}-V_{tl})]} \quad when\ V_{ds} > \frac{V_{gs}-V_{tl}}{P_{vf}} \quad (2)$$

$$I_{mosh} = (1-K_{fl})K_pK_f\frac{(V_{gs}-V_{th})V_{ds}-\frac{1}{y}\left[P_{vf}^{1-y}V_{ds}^{y}(V_{gs}-V_{th})^{2-y}\right]}{1+\theta(V_{gs}-V_{tl})} \quad (3)$$

$$when\ V_{ds} \le \frac{V_{gs}-V_{th}}{P_{vf}}$$

$$I_{mosl} = (1-K_{fl})K_p\frac{(V_{gs}-V_{th})^2}{2[1+\theta(V_{gs}-V_{th})]} \quad when\ V_{ds} > \frac{V_{gs}-V_{th}}{P_{vf}} \quad (4)$$

$$I_{MOS} = I_{mosl} + I_{mosh} \quad (5)$$

The MOSFET current equations have been represented in the PSpice code with two voltage-dependent current sources in parallel. Depending on the gate voltage and thresholds, an IF statement determines the operation of the device in linear or saturation region. The on-state resistance of the device is taken into account in the model as the series connection of the bulk (epitaxial layer) resistance, affected by the thickness of the drain-source depletion region and the carrier mobility, and a constant drain substrate resistance (Fig. 1). So the drain-source voltage Vdds is given by:

$$V_{dds} = V_{ds} + I_{MOS}(R_b + R_s) \quad (6)$$

In PSpice, a voltage-dependent voltage source has been connected in series with the MOSFET current to model the on-state drop. The switching behavior of the MOSFET is determined by the three capacitances in Fig. 1. In good approximation the gate-source capacitance is assumed to be constant, while the gate-drain and drain-source ones are dependent on the change of the respective depletion regions with the drain voltage. In particular, the gate-drain capacitance is considered as the series of the variable junction capacitance Cgdj and the fixed oxide capacitance Coxd. The correct estimation of these parameters implies the knowledge of the device area and oxide thickness, as well as other fundamental properties of the material. All the parameters of the depletion

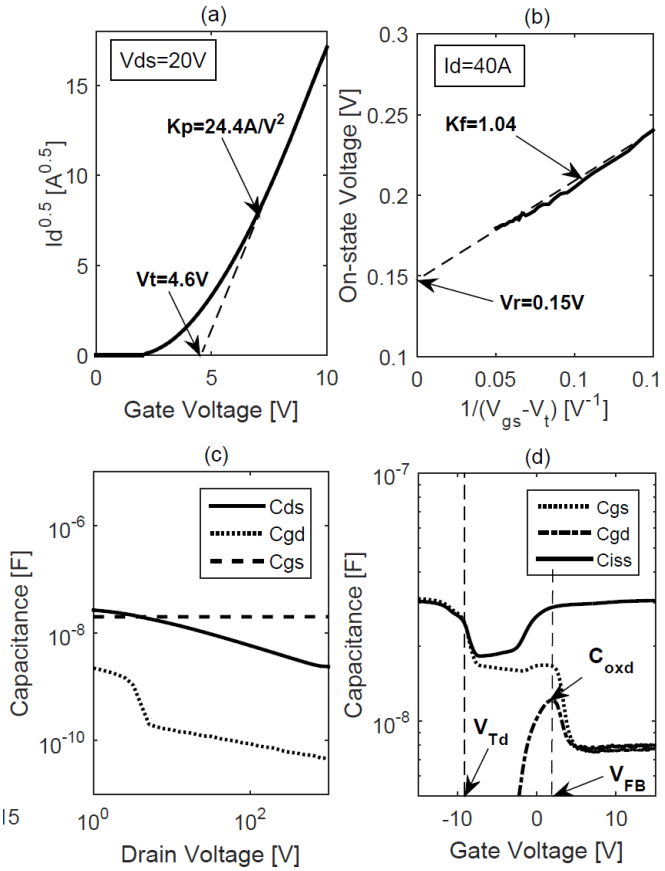

Fig. 3. Parameter extraction sequence: (a) saturation region; (b) linear region; (c)-(d) transient parameters

region (width, built-in voltage and carrier mobility) and the on-state resistance and capacitances values have been modeled in PSpice as stand-alone, voltage-dependent voltage sources. Both the drain capacitances are included in the code as voltage-dependent current generators. Moreover, the temperature dependency of threshold voltage Vt and saturation transconductance Kp is taken into account in the model through two simple behavioral equations (Eq. 7-8).

$$V_t = V_{t0} + V_{t1}(T_j - T_0) \tag{7}$$

$$K_p = K_{p0}\left(\frac{T_0}{T_j}\right)^{K_{p1}} \tag{8}$$

$$\mu_n = \frac{947}{1 + \left(\frac{N_b}{1.49 \cdot 10^{17}}\right)^{0.61}}\left(\frac{T_0}{T_j}\right)^{2.15} \tag{9}$$

Finally, the temperature dependency of the carrier mobility μ_n is also included, allowing the modeling of the on-state resistance Ron variation for high temperature (Eq. 9).

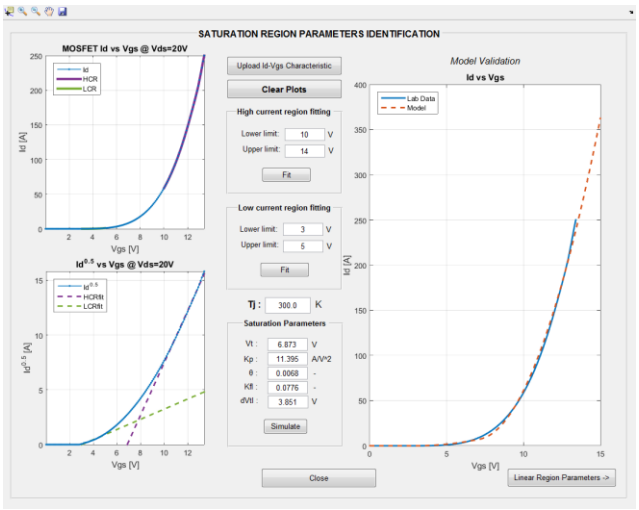

Fig. 4. MATLAB GUI panel for the identification of the saturation region parameters

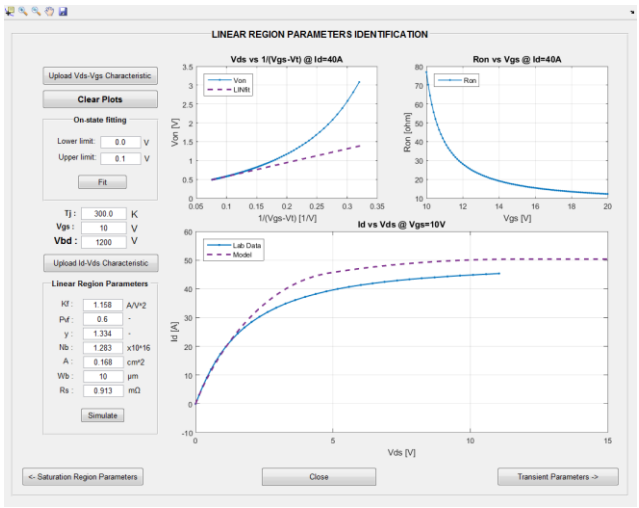

Fig. 5. MATLAB GUI panel for the identification of the linear region parameters

III. Parameter Extraction Procedure

The parameter extraction process proposed in [14] has been used for identifying the static parameters, while the method illustrated in [17] was adopted for the transient analysis. Other general-purpose equations related to semiconductor physical properties were also used [18], [19]. All the procedure has been embedded in a new "parameter-extraction tool" (see Fig. 2), developed in MATLAB through a GUI, consisting of three steps: saturation region, linear region and transient parameters identification [14]. Each of the steps has a dedicated panel in the GUI (Fig. 4 - 6), which allows the direct validation of the model, running the PSpice *.cir* simulation file and processing its output, together with the manual tuning of the extracted parameters. The main idea is to provide the user with a complete and rather simple tool to identify a given device/module and eventually create a PSpice model or library part without the need for advanced Spice programming effort.

The saturation region parameter extraction basically consists of an analysis of the I - V static characteristic of the device (Fig. 3.a). The extraction of gate threshold Vt and peak transconductance Kp is performed by fitting the high current region of the Id - Vgs curve for root squared values of Id, approximated as follows [14][20]:

$$\sqrt{I_d} = \sqrt{\frac{K_p}{2}}\,(V_{gs} - V_t) \tag{10}$$

Rearranging and manipulating the model equation it is possible to calculate the remaining coefficients.

The characteristic Vds - Vgs for a forced constant value of Id can be used to observe the on-state behavior and thus extract the linear transconductance Klin (and the linear transconductance factor Kf=Klin/Kp) and the on-state resistance. A fitting is easier to achieve when linearizing, plotting Vds = Von versus 1/(Vgs - Vt) instead of Vgs. The

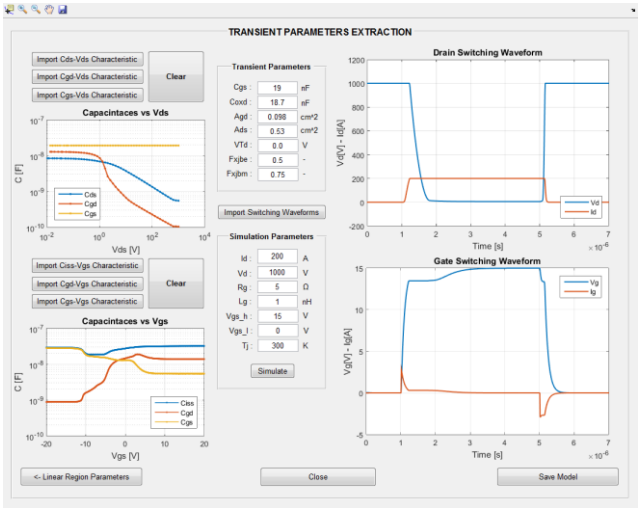

Fig. 6. MATLAB GUI panel for the identification of the transient parameters

TABLE I. EXTRACTED PARAMETERS

Parameter		Unit	Module 1 (Cree)	Module 2 (Microsemi)	Module 3 (Rohm)
Vbd	Module Rated Breakdown Voltage	kV	1.7	1.2	1.2
Id	Module Rated Drain Current	A	325	357	180
Vt	Gate Threshold Voltage	V	5.287	4.960	6.648
Kp	Saturation Transconductance	A/V^2	28.04	32.012	10.392
Kfl	Low Current Transconductance Factor	-	0.055	0.067	0.085
θ	Transverse Electric Field Parameter	-	0.001	0.005	0.006
dVtl	Low Threshold Voltage Difference	V	2.129	2.322	3.943
Kf	Linear Transconductance Factor	-	1.043	1.205	1.059
Rs	Drain Series Resistance	Ω	1.2	1.7	1.1
A	Active Area	cm^2	0.174	0.123	0.112
Nb	Bulk Doping Concentration	cm^{-3}	0.906×10^{16}	1.283×10^{16}	1.283×10^{16}
Wb	Bulk Thickness	µm	14	10	10
Pvf	Pinch-off Voltage Factor	-	0.65	0.65	0.45
Cgs	Gate-Source Capacitance	nF	20.05	15.43	20
Coxd	Oxide Capacitance	nF	12.14	12.34	12
Agd	Gate-Drain Depletion Area	cm^2	0.054	0.091	0.052
VTd	Gate-Drain Depletion Threshold	V	-9	-9	-11
Fxjbe	Depletion Charge Factor (edge)	-	0.5	0.5	0.5
Fxjbm	Depletion Charge Factor (middle)	-	0.75	0.75	0.75
TEMPERATURE DEPENDENCY PARAMETERS					
Vt0	Gate Threshold Temperature Coeff.	-	5.609	5.017	7.002
Vt1	Gate Threshold Temperature Coeff.	-	-0.0166	-0.0137	-0.0178
Kp0	Saturation Transconductance Temp. Coeff.	-	28.04	32.2	10.392
Kp1	Saturation Transconductance Temp. Coeff.	-	2	0.58	1

slope of this linear regression is inversely proportional to Klin (as expressed in Eq. 11). Through the value of the intercept Vr, rearranging Eq. 12, it is possible to find out Rb + Rs (Fig. 3.b).

$$V_{on} = V_r + \frac{I_d}{K_{lin}(V_{gs} - V_t)} \qquad (11)$$

$$V_r = I_d(R_b + R_s) + \frac{I_d\theta}{K_{lin}} \qquad (12)$$

The estimation of the depletion region parameters is carried out following some simple equations related to the breakdown voltage and the intrinsic properties of 4H-SiC material [18], including the identification of the device active area A. The identification of the device transient parameters is made

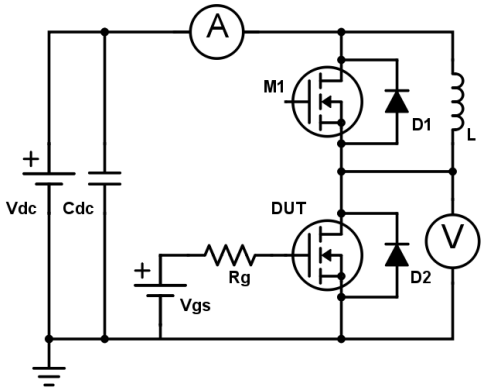

Fig. 7. Schematic of the double-pulse switching test setup.

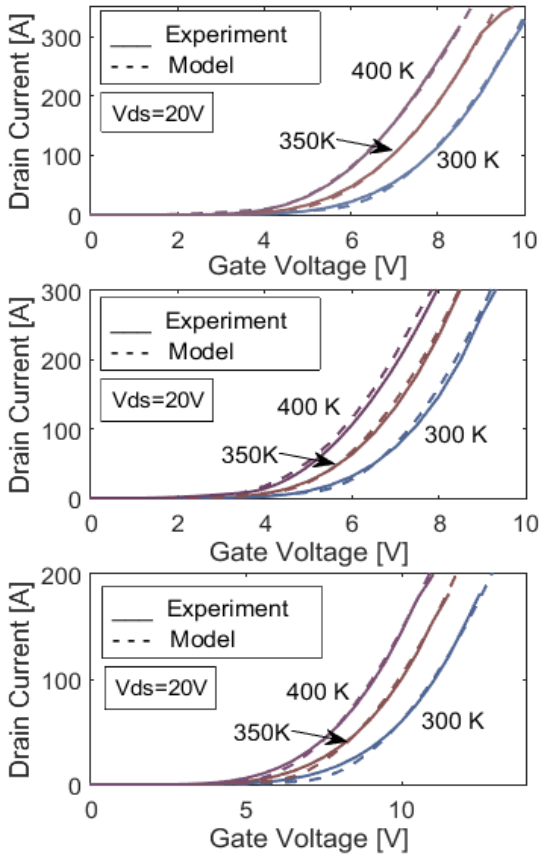

Figure 8. Id-Vgs validation with temperature spread for three modules: Cree (top), Microsemi (middle), Rohm (bottom).

through the study of the capacitance variation over drain voltage (carrying out measurements up to Vds=1.0 kV, with Vgs=0) and gate voltage sweep (from -20 V to 20 V, with Vds=0). In particular, from Cds-Vds and Cgd-Vds, it is possible to estimate the respective depletion overlap regions areas [17], while the mean value of Cgs-Vds gives the constant gate-source capacitance (Fig 2.c). Cgd-Vgs sweep allows instead to find out the value of Coxd, correspondent to the flat band voltage V_{FB} (depletion region is negligible and Vgs drops only on the SiO_2 insulator), and the depletion threshold V_{Td} (Fig 2.d) [17]. The proposed parameter identification strategy has only been applied to single-die devices in the literature so far, though the model validation shows its rather good suitability when applied to high-power multi-chip modules.

IV. Experimental Results and Validation

The whole experimental and theoretical work has been carried out at ABB Corporate Research Center in Västerås, Sweden. A power device curve tracer (i.e., B1505A from Keysight) was used to obtain the static characteristics and the capacitance measurements with a rather simple experimental setup. For the switching measurements, a double pulse test has been set up in a circuit with inductive load. Two devices of the same type have been used in the circuit: one as DUT and the other to provide freewheeling path for the current through its body diode, as shown in Fig. 7. A similar setup was used for the parallelization of two devices of the same type. A hot plate with temperature regulation was used to heat up the DUT up to 425 K and measure the static and dynamic parameters spread. Different load inductances values and DC bus voltage levels have been set when performing the measurements. The gate drive unit (GDU) provides option to vary the gate resistance as well. The room temperature parameters extracted by means of the presented procedure and the temperature dependency coefficients for Vt and Kp are listed in Table I for the three tested modules.

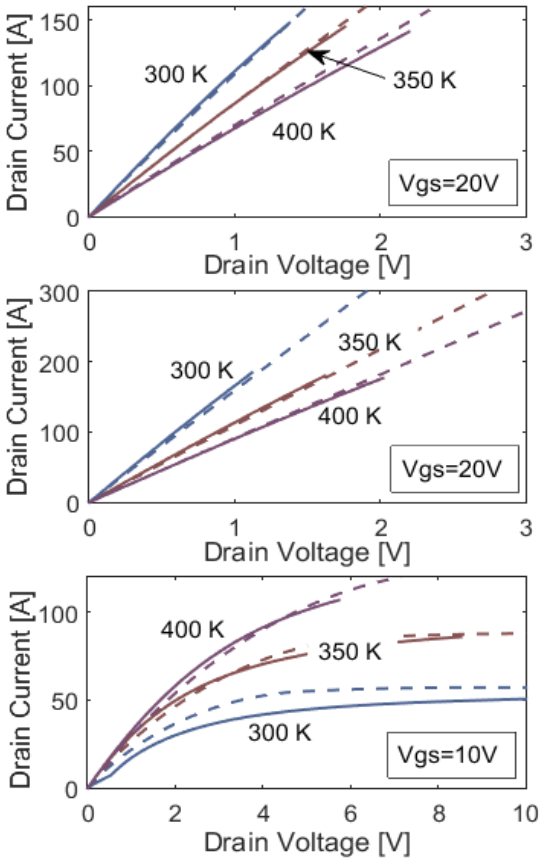

Figure 9. Id-Vds validation (solid: exp; dashed: model) with temperature spread for three modules: Cree (top), Microsemi (middle), Rohm (bottom).

Table III. Switching Tests Results

Parameter	Unit	Module 1 (Cree)	Module 2 (Microsemi)	Module 3 (Rohm)
T	K	300	300	300
V_{DC}	V	1000	800	900
I_{load}	A	200	100	200
Lσ	nH	30	150	50
Rg	Ω	10	15	10
Vdds	V	965	790	879
$V_{OS\%}$	-%	11.8 (15)	27.1 (32.1)	20.6 (18.5)
$I_{OS\%}$	-%	33.5 (31)	40 (47)	13 (15.3)
Eon	mJ	16.2 (20)	8.1 (7.6)	17 (18.9)
Eoff	mJ	25.9 (23.1)	9.3 (11)	22.7 (24.1)
Etot	mJ	42.1 (43.1)	17.4 (18.6)	39.7 (43)

A. Static Validation

In Fig. 8-9, the results of the validation for the static I-V characteristic have been reported. The curves have been simulated and compared with experimental data at different temperature values. A satisfactory agreement is achieved over different bias conditions with relative error rarely exceeding 5%. In particular, the model succeeds in taking into account the degradation of carrier mobility for high gate voltages at high temperature, which is a rather important property in SiC devices, preventing thermal runaway during fault conditions and self-stabilizing the device. The coefficients used for the temperature dependency modeling of Vt and Kp result from behavioral fittings of the experimental curves. Moreover, the variation of on-state resistance Ron with temperature in the model has been experimentally validated for the three modules, resulting in a good matching, shown in Fig. 10.

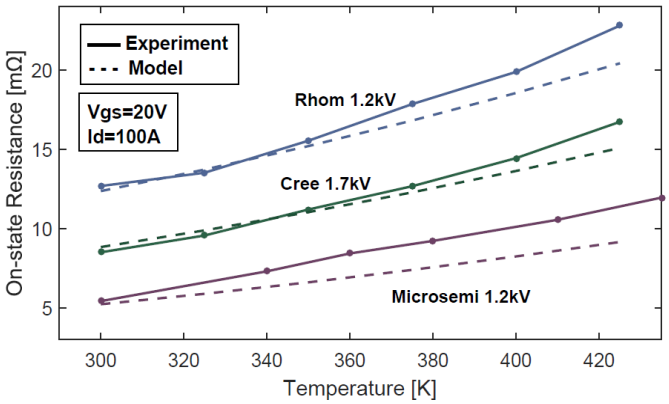

Fig. 10. Ron variation with temperature for three modules with model validation

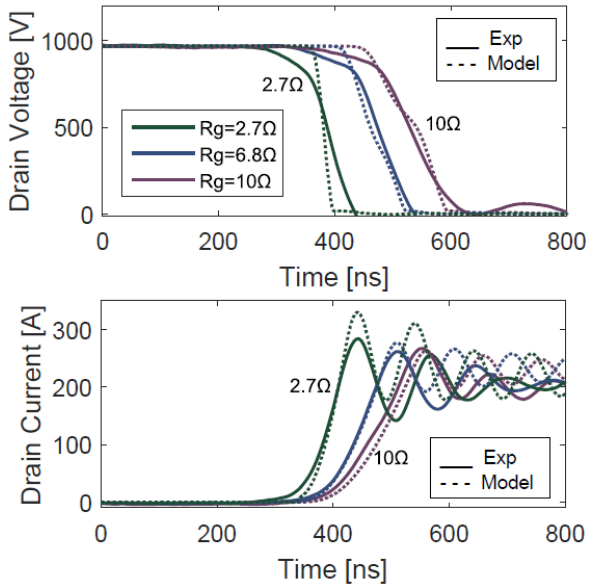

Figure 11. Validation of turn-on switching waveforms (Solid: exp, Dotted: model) for Cree module with Rg spread of 2.7, 6.8 and 10 Ω.

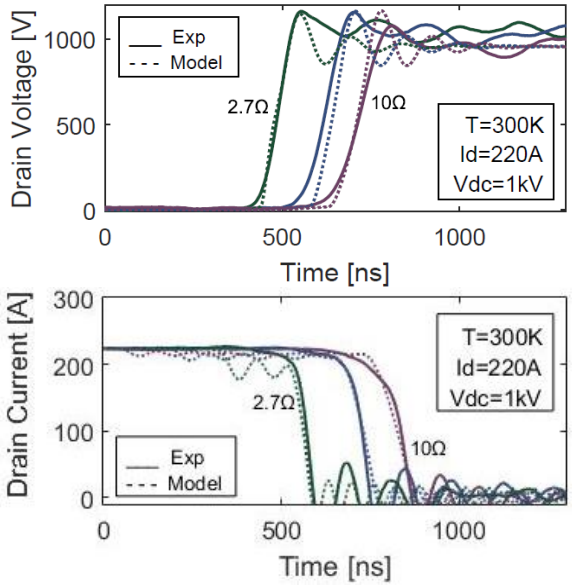

Figure 12. Validation of turn-off switching waveforms (Solid: exp, Dotted: model) for Cree module with Rg spread of 2.7, 6.8 and 10 Ω.

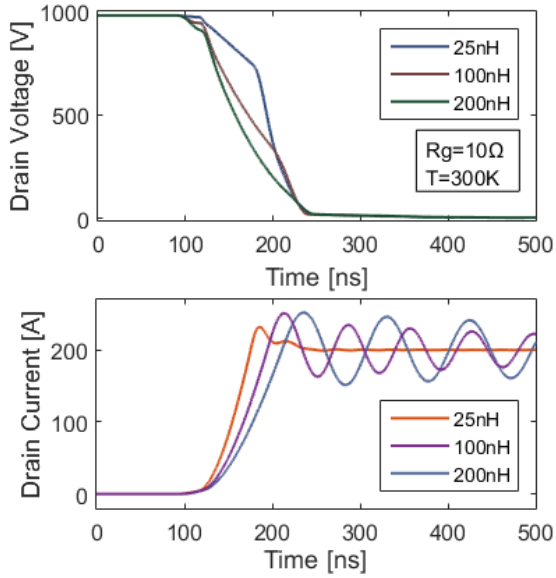

Fig. 13. Simulated turn-on switching waveforms for Cree module with Lσ spread of 25, 100 and 200 nH.

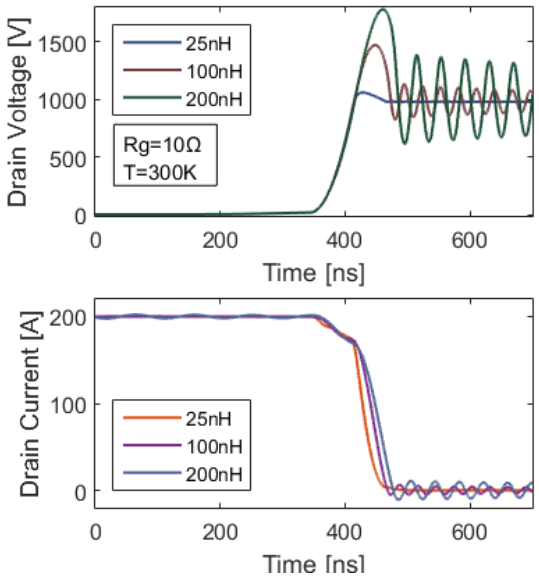

Fig. 14. Simulated turn-off switching waveforms for Cree module with Lσ spread of 25, 100 and 200 nH.

B. Dynamic Validation

The results of a transient simulation, compared with switching measurements, are showcased in Fig. 11 - 12 for the Cree 1.7kV-325A module for three different gate drive resistances. Here, the model predicts fairly well the switching behavior of drain voltage and current during both turn-on and turn-off transients, though parasitic elements had to be included in the simulation to imitate the oscillation's amplitude and frequency given by the stray elements present in the module and in the setup itself. Table II reports the values of DC bus voltage V_{DC}, load current I_{load}, loop stray inductance Lσ (extracted from the measurements), and gate resistance Rg used during the tests as well as the drain voltage measured value (after the drop) Vdds, the turn-on overshoot for voltage and current and the switching energy losses compared with the model estimation (values in brackets).

No significant variation of the switching behavior at high temperatures was noticed. Further analysis have been carried out for both circuit and intrinsic parameter spread in order to define a range of reliability for the model and its estimation capability of switching losses. Lσ was changed in the switching-mode simulations, showing the expected behavior. As shown in Fig. 13 and 14, an increase in the rise and fall time can be noticed for higher values of Lσ. On the other side, the transient frequency is reduced while the turn-off voltage overshoot and the oscillation amplitude becomes higher. The switching energy losses variation is plotted in Fig. 15 with Lσ

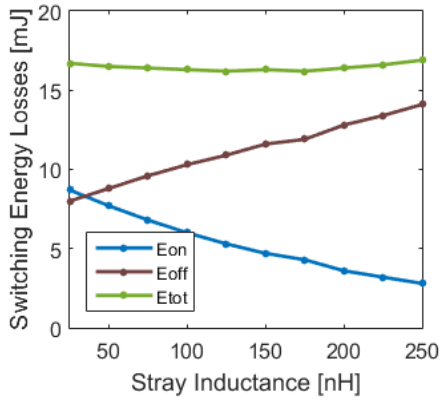

Fig. 15. Simulated switching energy losses vs. stray inductance for Cree 1.7kV module

from 25 nH to 250 nH. Here, two opposite phenomena are occurring: during turn on the slower current and voltage transients provoke decreasing losses for higher Lσ; on the other hand, during turn off the increased overvoltage results in higher losses. The two effects cause the overall losses in the device to remain almost unchanged for higher stray inductance, as visible in Fig. 15.

C. Current Sharing Analysis

Accurate studies about parallel SiC MOSFETs have been carried out in [21] - [23] and an active current balancing has been proposed in [24]. The focus of these studies has been the observation of static and dynamic characteristics of the parallel modules or devices in order to figure out and quantify how the mismatches in the module's characteristics can influence the switching behavior. Fig. 16 shows one of the experimental results for the double-pulse test carried out on

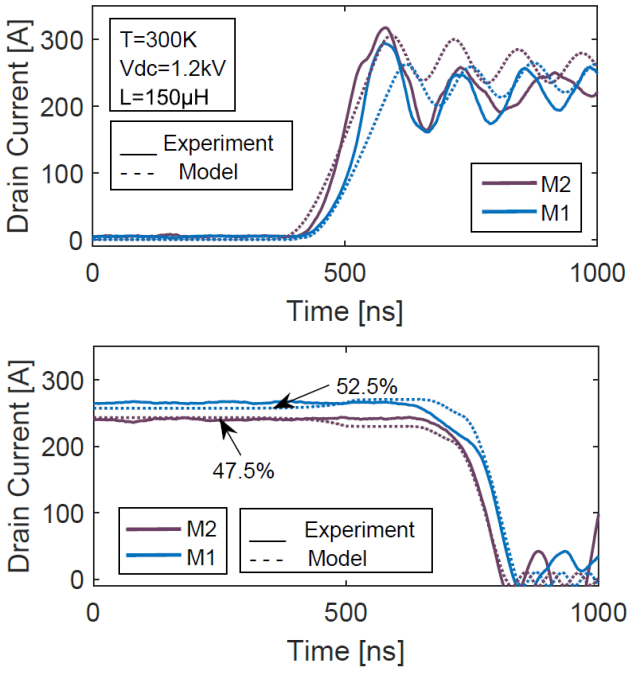

Fig. 16. Current sharing for two paralleled 1.7kV Cree modules during turn-on and turn-off with model validation

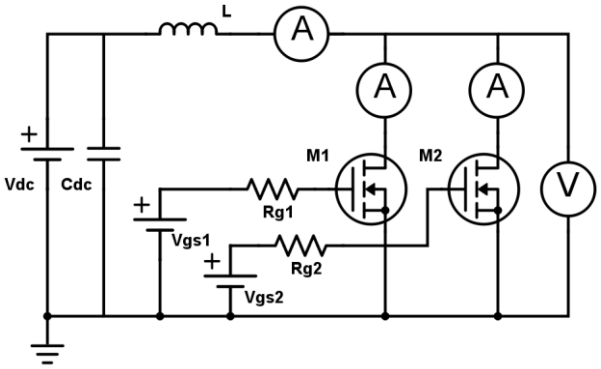

Fig. 17. Measurement setup for double-pulse test of two parallel connected modules

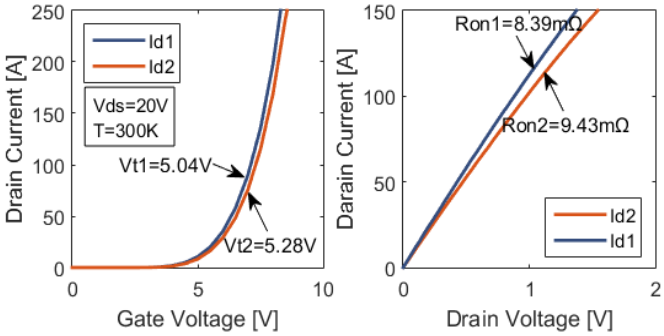

Fig. 18. Mismatch between the static characteristics for two Cree 1.7kV modules

two parallel 1.7 kV modules with the setup reported in Fig. 17, and the related modeling. The model parameters are different for the two devices and have been extracted carrying out separate static measurements on each module in order to properly identify the mismatch, which in this case is not particularly relevant, as visible in Fig. 18. Module M1 presents slightly bigger gate threshold and smaller on-state resistance than M2 and this affects the current sharing and the switching speed. In particular, it can be observed from Fig. 16 that M1, as expected, carries less current in comparison to M2; so does it happen in the simulation. The shift of the two waveforms during switching can be due to several phenomena, including gate resistance mismatch and gate pulse delay. The model, however, successfully represents with satisfactory precision the unbalances, though the influence of the stray elements has to be investigated further [21]. In the simulated circuit, the drain stray inductances were kept at the same value for both the modules. A mismatch in the gate resistances was introduced to simulate the delay of the waveforms. It can be observed that the current sharing is accurately modeled, while the transient dynamics still show some inaccuracy, especially in the turn-on transient, though the delay is correctly estimated.

V. Conclusions

This work presents a deep investigation on the modeling approach and parameter identification for SiC MOSFETs, through solid but simplified implementation strategy. The implemented model combined with the exposed identification method is capable of simulating in a wide range of operational

conditions the behavior of three different MOSFET multichip modules, as showed in the experimental validation. Moreover, the simulation time for one switching period of about 5µs, solved by a variable step-size algorithm with 0.1 ns maximum step, took less than one minute to be worked out, which makes this implementation very suitable for simulating more complex topologies, with several connected modules. The model has been proven to be robust and convergent in all the analyzed operating conditions. Furthermore, an insight into the parallel connection of SiC power modules has been gained, enabling a good correlation between the different modules' characteristics and the switching unbalances. A dedicated and complete MATLAB GUI has been created in order to easily identify the model parameters and obtain a turn-key simulation file and/or an editable PSpice model. The implemented model is capable of properly simulating the forward biasing operation of the device, yet further improvements for this work are: 1) the reverse conduction region modeling; 2) the body diode modeling; 3), the breakdown behavior modeling; 4) the short circuit thermal modeling. An improved and complete model should therefore include these features, which is the objective of our future research. In addition, an improved thermal modeling can be introduced, whose output is the junction temperature based on the energy losses of the device.

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